What is claimed is:

1. A method of manufacturing a semiconductor device having a thyristor and a substrate with an upper surface, the method comprising:

forming a thyristor having a body and a control port capacitively coupled to the thyristor body, the body including an emitter region below the upper surface of the semiconductor substrate; and

forming a conductive shunt in the substrate and extending between a node at the upper surface of the substrate and the emitter region.

2. The method of claim 1, further including:

forming a pass device having first and second source/drain regions separated by a channel region and a gate capacitively coupled to the channel region, the first source/drain region being electrically coupled to the emitter region via the node at the upper surface of the substrate.

3. The method of claim 2, wherein forming a conductive shunt comprises:

etching a trench in the substrate and adjacent to the emitter region;

lining the trench with an electrically insulative material; and

forming a conductive shunt material in the trench and electrically coupled to the emitter region and to the first source/drain region.

4. The method of claim 3, wherein forming a thyristor having an emitter region in the substrate includes implanting the emitter region via a bottom portion of the trench, prior to forming the conductive material in the trench.

5. The method of claim 3, further including removing a portion of the liner at a bottom of the trench, prior to forming the conductive material in the trench, wherein forming a conductive material in the trench and electrically coupled to the emitter region includes forming the conductive material electrically coupled to the emitter region via a portion of the trench where the liner has been removed.

6. The method of claim 3, wherein etching a trench in the substrate and adjacent to the emitter region includes etching a trench around a portion of the thyristor.

7. The method of claim 6, wherein forming a thyristor having a body and a control port includes forming the control port in the trench, further including forming insulative material in the trench and between the control port and the conductive shunt, the insulative material being configured and arranged to electrically insulate the conductive shunt from the control port.

8. The method of claim 3, wherein lining the trench with an electrically insulating material comprises:

filling the trench with the electrically insulating material; and

removing a portion of the electrically insulating material from the trench and thereby forming a lined trench.

9. The method of claim 8, wherein removing a portion of the electrically insulating material includes exposing a portion of a bottom of the trench and wherein forming a conductive material in the trench and electrically coupled to the emitter region includes forming the conductive material electrically coupled to the emitter region via the exposed portion of the bottom of the trench.

10. The method of claim 3, wherein etching the trench includes etching a trench extending into the emitter region.

11. The method of claim 3, wherein forming a conductive material in the trench includes depositing polysilicon in the trench and subsequently doping the deposited polysilicon.

12. The method of claim 3, further including etching a shallow trench isolation (STI) region in the substrate, prior to etching the trench adjacent to the emitter region, wherein etching the trench adjacent to the emitter region includes etching a portion of the substrate below the STI region and using said portion of the substrate below the STI region to inhibit lateral diffusion of the conductive shunt material.

13. The method of claim 3, wherein etching a trench in the substrate and adjacent to the emitter region includes etching a trench having a varied depth with a greater depth below the STI region, relative to portions of the trench not below the STI region.

14. The method of claim 3, wherein forming a thyristor comprises:

forming a trench in the substrate;

implanting the emitter region via a bottom portion of the trench;

forming a first base region in a portion of the substrate adjacent to the trench and electrically coupled to the emitter region;

forming a second base region electrically coupled to the first base region;

forming a second emitter region electrically coupled to the second base region; and

forming a control port in the trench and capacitively coupled to at least one the first base region and adapted to form a conductive channel between the emitter regions in response to a voltage being applied thereto.

15. The method of claim 14, wherein forming the control port comprises:

forming a dielectric on a sidewall of the trench; and

forming the control port in the trench and capacitively coupled to at least one of the first and second base regions via the dielectric.

16. The method of claim 15, wherein forming a trench includes forming a trench around a portion of the substrate including the first base region and wherein forming the

control port and forming the conductive shunt includes forming the control port and the conductive shunt in different portions of the same trench and electrically isolating the control port from the conductive shunt.

17. The method of claim 1, further including out diffusing material from the conductive shunt to form the emitter region.

18. A method of manufacturing a semiconductor device including a substrate having an upper surface, the method comprising:

forming a vertical thyristor in the substrate, the vertical thyristor including a thyristor body and a control port, the body having an N+ emitter region in the substrate and below the upper surface, a P base region on the N+ emitter region, an N base region on the P base region and a P+ emitter region on the N base region, the control port being separated from the P base region by a dielectric and configured and arranged to capacitively couple a signal to the P base region via the dielectric in response to a voltage applied thereto for controlling current flow in the thyristor;

forming an N+ conductive shunt electrically connected to the N+ emitter region and extending between the N+ emitter region and the upper surface; and

forming a pass device having first and second N+ source/drain regions separated by a channel region and a gate capacitively coupled to the channel region, the first N+ source/drain region being coupled to the conductive shunt.